REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. The foregoing amendments are responsive to the August 1, 2001 Office Action. Applicants respectfully request entry of the requested amendments and reconsideration of the application in view of the following comments.

Response to objections under 35 U.S.C. § 112, second paragraph

Claims 3-6, 11-12, 17, 23, and 65-67 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Applicants amend the claims herein to correct any indefiniteness and Applicants respectfully submit that all claims now comply with the requirements of 35 U.S.C. § 112.

Response to the Claim Rejections Under 35 U.S.C §§ 102 and 103

Claims 9, 10. 18-24, 26, 29, 30, 32, 35-37, 39, 42-44, 46, 49-51, 53, 56, 57, 58, 60, 63, and 64 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,236,064 issued to Mase, et al. The rejection asserts that Mase allegedly teaches each element of the claims. Claims 1 and 2 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mase in view of U.S. Patent No. 5,585,658 issued to Mukai, et al. The

rejection asserts that Mase allegedly teaches each element of the claims except for the impurity region formed through a resist mask, which is allegedly taught by Mukai. Claims 7 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent No. 404,186,775a issued to Yamazaki. The rejection asserts that Yamazaki allegedly teaches each element of the claims except for implanting an oxygen ion into a crystal semiconductor by electron beam, which is allegedly obvious to one of skill in the art. Claims 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Mukai. The rejection asserts that Yamazaki allegedly teaches each element of the claims except patterning the resist by a FIB method, which is allegedly taught by Mukai. Claims 13 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mase.. The rejection asserts that Mase allegedly teaches each element of the claims except for the intervals and impurity regions that alternate with the intervals in a direction of a channel width of the channel forming region, which is allegedly obvious to one of skill in the art. Claims 25, 27, 31, 33, 38, 40, 45, 47, 52, 54, and 59 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mase. The rejection asserts that Mase allegedly teaches each element of the claims except for the intervals and impurity regions that alternate with the intervals

in a direction of a channel width of the channel forming region, which is allegedly obvious to one of skill in the art.

One embodiment of present invention, as described in the specification, is directed toward forming an intrinsic or substantially intrinsic region and an impurity region in a channel forming region. A carrier moves through the intrinsic or substantially intrinsic region while the carrier avoids the impurity region formed in the channel forming region.

None of the cited art teaches or suggests the present invention. Mase states in column 5 that it is advantageous to implant oxygen, carbon, or nitrogen ions into only parts of the channel formation regions. However, Mase does not suggest that a carrier moves through a channel forming region while the carrier avoids the parts of the channel formation regions implanted with oxygen, carbon, or nitrogen. Therefore, the reference to Mase does not suggest that a carrier moves through the intervals or substantially intrinsic region while the carrier avoids the impurity region formed in the channel forming region.

Yamazaki states that oxygen is intentionally added to channel forming regions 7 and 7'. However, Yamazaki does not suggest that a carrier moves through a channel forming region while the carrier avoids a region added with the oxygen.

Therefore, Yamazaki does not suggest that a carrier moves through the intrinsic or substantially intrinsic region while the carrier avoids the impurity region formed in the channel forming region.

In view of the foregoing distinctions, Applicants respectfully submit that amended independent Claims 1, 7, 9, 13, 15, and 18-23 are patentably distinguished over the cited art. Applicants respectfully submit that Claims 1, 7, 9, 13, 15, and 18-23 are in condition for allowance, and Applicants respectfully request allowance of Claims 1, 7, 9, 13, 15, and 18-23.

Claims 2, 8, 10, 14, 16, 24-64, and 68-73 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding Claims 1, 7, 9, 13, 15, and 18-23, Applicants respectfully submit that Claims 2, 8, 10, 14, 16, 24-64, and 68-73 are likewise in condition for allowance. Applicants respectfully request allowance of dependent Claims 2, 8, 10, 14, 16, 24-64, and 68-73.

Allowable Subject Matter

Claims 3-6, 11-12, 17, and 65-67 are indicated to contain allowable subject matter if rewritten to overcome the rejections under 35 U.S.C. § 112. Applicant has amended Claims

3, 5, 11, 17, and 66 to overcome the 35 U.S.C. § 112 rejection to Claims 3-6, 11-12, 17, and 65-67, and therefore Applicant respectfully requests allowance of Claims 3-6, 11-12, 17, and 65-67.

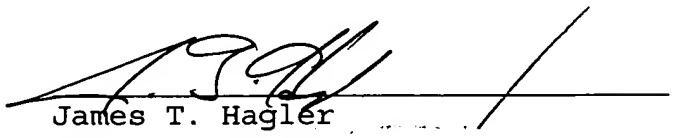
Summary

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Applicant asks that all claims be allowed. Enclosed is a $508.00 check for excess claim fees and for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/28/01



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Version with markings to show changes made

In the claims:

Claims 68 - 73 have been added.

Claims 1, 3, 5, 7, 9, 11, 13, 15, 17, 18, 19, 20, 21, 22 23, and 66 have been amended as follows:

1. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming [a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, the step of forming said plurality of impurity regions being conducted] an intrinsic or substantially intrinsic region and an impurity region in said part to become the channel forming region by introducing a first impurity [thereinto] into said impurity region through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel forming region.

3. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region:

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide[, wherein said impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region].

5. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said

thermal oxide and to make said boron segregated in said thermal oxide[,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region].

7. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

forming an intrinsic or substantially intrinsic region and an oxide region in said part to become the channel forming region by thermally treating said crystal semiconductor comprising silicon to change a region [thereof] of said crystal semiconductor implanted with said oxygen ion by said implanting step into [an] said oxide region [which forms a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region]; and

introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said oxide region formed in said part to become the channel forming region.

9. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming an intrinsic or substantially intrinsic region and an impurity region in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into [a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region] said impurity region, said [plurality of] impurity [regions] region containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel forming region.

11. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

[wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, and]

wherein said impurity is added by said adding step to said substrate to a depth deeper than an etched depth formed in said groove-like or hole-like pattern by said anisotropic etching.

13. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

[introducing a first impurity into a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which form a dotted pattern in said part to become a channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region,]

<u>forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity regions,</u> said plurality of impurity regions containing an element selected from the group

consisting of carbon, nitrogen and oxygen as said first impurity;

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein [said channel forming region includes intervals, and] said impurity regions [alternates] alternate with said [intervals] intrinsic or substantially intrinsic region in a direction of a channel width W of said channel forming region, and

wherein said impurity regions have total width of Wpi in a direction of said channel width W, and a total width of said [intervals] intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9.

15. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming [a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, the step of forming said plurality of impurity regions being conducted] an intrinsic or substantially intrinsic region and a plurality of impurity regions in said part to become the channel forming region by introducing a first impurity

[thereinto] into said impurity regions through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein [said dotted pattern has an arrangement in which] said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said part to become the channel forming region.

17. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions [which form a dotted

pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, and]

wherein [said dotted pattern has an arrangement in which] said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

18. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode [on] over said channel forming region[; and];

[in said channel forming region, forming a region in which carriers move, and impurity regions which pin a depletion layer that expands from said drain region toward said channel forming region and said source region, artificially and locally]

wherein said impurity region formed in said channel forming region pins a depletion layer that expands from said drain region toward said channel forming region and said source region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

19. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region;

forming a gate insulating film and a gate electrode [on] over said channel forming region[; and],

[in said channel forming region, forming a region in which carriers move, and impurity regions which controls the threshold voltage to a predetermined value voltage by the addition of impurity elements, artificially and locally]

wherein said impurity region controls the threshold voltage to a predetermined value voltage, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

20. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity [regions] region [artificially and locally] in said channel forming region; and

forming a gate insulating film and a gate electrode [on] over said channel forming region,

wherein an impurity [elements] element that expand an energy band width (Eg) [are artificially and locally] is added to said impurity [regions] region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

21. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode [on] over said channel forming region[; and],

[in order to form impurity regions which pin a depletion layer that expands from said drain region toward said channel forming region and said source region, artificially and locally adding impurity elements that expand an energy band width (Eg) to said channel forming region]

wherein said impurity region pins a depletion layer that expands from said drain region toward said channel forming region and said source region,

wherein an impurity element that expands an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

22. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode [on] over said channel forming region[; and],

[in order to form impurity regions which control the threshold voltage to a predetermined value voltage by addition of impurity elements, artificially and locally adding impurity elements that expand an energy band width (Eg) to said channel forming region]

wherein said impurity region controls the threshold voltage to a predetermined value voltage,

wherein an impurity element that expand an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

23. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

[artificially and locally forming impurity regions by addition of impurity elements that expand an energy band width (Eg) in said channel forming region; and]

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode [formed on] over said channel forming region,

wherein said impurity [regions have] region has an insulating property, [and

wherein said impurity elements are not added or are added by a very small amount in a region other than said impurity regions in said channel forming region]

wherein an impurity element that expands an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region.

66. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions [which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region,]

wherein [said dotted pattern has an arrangement in which] said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.